In the Claims:

1. (Currently Amended) An ~~buffer of an~~ integrated circuit (IC) having ~~the~~a buffer located therein for reducing delays on relatively long conductive signal lines of the IC, the buffer comprising:

a first inverter having an input connected to one of said conductive signal lines of the~~an~~ IC ~~that comprises the buffer~~;

a second inverter having an input connected to an output of the first inverter of the IC; and

a protection diode connected to the input of the first inverter, the protection diode pulling at least some electrical charge off at least one gate of at least one transistor of the first inverter to prevent the buffer from being damaged by too much electrical charge collecting on the transistor gate.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The IC~~buffer~~ of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on the area of the transistor gate.

5. (Currently Amended) The ~~buffer~~IC of claim 1, wherein the first and second inverters each comprise a P field effect transistor (PFET) and an N field effect transistors (NFETs).

6. (Currently Amended) The ~~buffer~~IC of claim 1, wherein each inverter comprises at least ~~one~~ a first bipolar junction transistor ~~(BJT)~~.

7. (Currently Amended) The ~~buffer~~IC of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal line to which the input of the first inverter is connected.

8. (Currently Amended) The ~~buffer~~IC of claim 1, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the input of the first inverter is connected and on the gate area of said transistor gate of the first inverter.

9. (Currently Amended) The ~~buffer~~IC of claim 1, wherein the size of the protection diode in terms of area depends at least partially on the IC process used to design the IC.

10. (Currently Amended) A method for preventing buffers used to reduce delays on relatively long conductive signal lines of an IC from being damaged due to electrical charges that collect on the buffers during manufacturing of the IC, the method comprising the steps of:

buffering at least one conductive signal line of an IC with a buffer to reduce delays in the conductive signal line, said buffer comprising first and second inverters, the first and second inverters, the buffer including a protection diode connected to an input of the first inverter, the protection diode pulling at least some of the electrical charge off of at least one gate of at least one transistor of the first inverter to prevent the buffer from being damaged by too much electrical charge collecting on said transistor gate, the buffer and the protection diode being contained in the IC.

11. (Previously Amended) The method of claim 10, wherein the buffering step includes buffering multiple conductive signal lines of the IC with buffers, and wherein every buffer of the IC comprises first and second inverters and a protection diode connected to an input of the first inverter.

12. (Previously Amended) The method of claim 10, further comprising the step of determining whether a buffer needs a protection diode prior to buffering one of said conductive signal lines with a buffer that includes a protection diode.

13. (Previously Amended) The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on the gate area of said transistor.

14. (Original) The method of claim 10, wherein the size of the protection diode in terms of area is preselected.

15. (Currently Amended) The method of claim 10, wherein the IC is manufactured using a bipolar junction transistor process technology.

16. (Previously Amended) The method of claim 10, wherein the IC is manufactured using field effect transistor process technology.

17. (Previously Amended) The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal.

18. (Previously Amended) The method of claim 10, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the buffer input is connected and on the gate area of said transistor.

19. (Original) The method of claim 10, wherein the size for the protection diode in terms of area depends at least partially on the IC process used to design the IC.

20. (Original) The method of claim 11, wherein the size for the protection diode in terms of area is preselected.

21. (Currently Amended) A method for use in designing an integrated circuit (IC) comprising:

inserting buffer cells into an IC design such that respective inputs of the respective buffer cells are connected to conductive signal lines of the IC design for reducing delays on the conductive signal lines, each buffer cell including:

first and second inverters, the first and second inverters each having at least a non-inverting transistor and an inverting transistor with gates electrically coupled together, an output of the first inverter being connected to an input of the second inverter; and

a protection diode connected to an input of the first inverter inside of the IC.